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Parametric Macromodels of Differential Drivers With Pre-Emphasis

Igor S. Stievano, *Member, IEEE*, Ivan A. Maio, *Member, IEEE*, Flavio G. Canavero, *Senior Member, IEEE*, and Claudio Siviero

***Abstract*—This paper discusses the extraction of behavioral models of differential drivers with pre-emphasis for the assessment of signal integrity and electromagnetic compatibility effects in multigigabit data transmission systems. A suitable model structure is derived and the procedure for its estimation from port transient waveforms is illustrated. The proposed methodology is an extension of the macromodeling based on parametric relations applied to plain differential drivers. The obtained models preserve the accuracy and efficiency strengths of behavioral parametric macromodels for conventional devices. A realistic application example involving a high-speed communication path and a 3.125 Gb/s commercial driver model with pre-emphasis is presented.**

***Index Terms*—Circuit modeling, digital integrated circuits, electromagnetic compatibility, macromodeling, signal integrity, system identification.**

I. Introduction

NOWADAYS, a cost effective solution for the transmission of signals in the gigabyte per second range relies on the preconditioning of signals sent on data links made of conventional interconnects. Preconditioning is aimed at enhancing the high-frequency components of the transmitted signals, in order to compensate for the low-pass distortion effect introduced by the interconnects. These techniques arise from communication and signal processing theory and give rise to driver devices with pre-emphasis features as well as to sophisticated solutions based on channel equalization. High-performance differential data links based on these solutions have been successfully demonstrated in [1]–[4].

Signal conditioning adds to the increasing complexity of present driver and receiver circuits, and demands for accurate and efficient models to be used in system-level simulations aimed at the assessment of data link performance and signal integrity effects.

In this study, the state-of-the-art $\mathrm{M}\pi\log$ (Macromodeling via Parametric Identification of LOgic Gates) approach for the behavioral modeling of digital devices is extended to this class of devices [11]. The $\mathrm{M}\pi\log$ approach relies on the theory of system identification that is widely applied to the approximation of nonlinear dynamic systems (examples are industrial plants, mechanical systems, economic trends, etc.) and has proved to be effective for the derivation of behavioral models of digital drivers and receivers [7], [8]. The proposed macromodels are expressed in terms of suitable nonlinear parametric relations, that can be easily estimated from device port responses and can be readily converted into SPICE-like subcircuits or directly implemented as metalanguage descriptions, like VHDL-AMS.

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II. Device and Model Structure

In this section, a basic scheme of a driver circuit with pre-emphasis is considered and a suitable model structure whose parameters can be effectively estimated from device port transient responses only is presented.

In order to describe the main blocks composing a differential driver of this class, the principles of pre-emphasis are first introduced through a simple example taken from signal processing theory. We start by considering a generic bit stream defined by a discrete-time sequence $x(k)$, $k = 1,2,\ldots,x \in \{0,1\}$, that must be sent on the interconnect. Losses and dispersion on transmission lines have a low-pass effect, thus requiring an enhancement of the high-frequency components of the transmitted signal. A common approach is to apply a finite impulse response (FIR) filter to the original sequence $x(k)$ in order to produce a new transmitted sequence, named $y(k)$. Without loss of generality, the simplest FIR filter with two coefficients writes

$$y(k) = a_1 x(k) + a_2 x(k-1) \tag{1}$$

whose transfer function in the z domain is $H(z) = a_1 + a_2 z^{-1}$, and the frequency response turns out to be $H(\omega) = a_1 + a_2 \exp(-j\omega T)$, where T is the pulse width. As an example, Fig. 1 shows the spectrum $|Y(j\omega)|$ of the transmitted sequence $y(k)$ for a bit stream $x(k) =$ "011010." The pulse width is set to $T = 1$ ns and the filter coefficients are $a_1 = 1, a_2 = -\beta$; two different values of β are considered, i.e., $\beta = 0$ (no emphasis) and $\beta = 0.33$ (33% of emphasis). Fig. 1 highlights the effect of the FIR filter enhancing the frequency components of the transmitted signal in the range [0.2, 0.8] GHz.

A suitable design of the filter, i.e., the tuning of the filter coefficients a_1, a_2 of (1) leads to the optimal transmitted signal compensating for the frequency attenuation of the interconnect (i.e., of the communication channel), thus providing good quality received signals. A discussion of tuning of the filter coefficients is out of the scope of the present paper, but can be found in [13].

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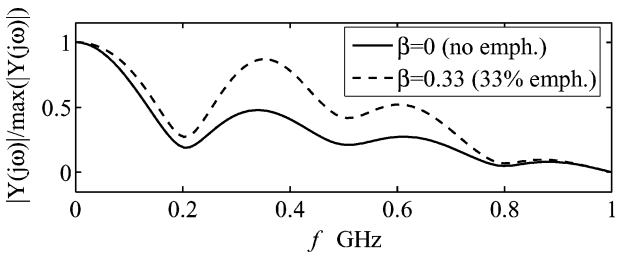

Fig. 1. Example spectra of $y(k)$ signal [see text and (1)] for no emphasis (solid line) and 33% emphasis (dashed line).

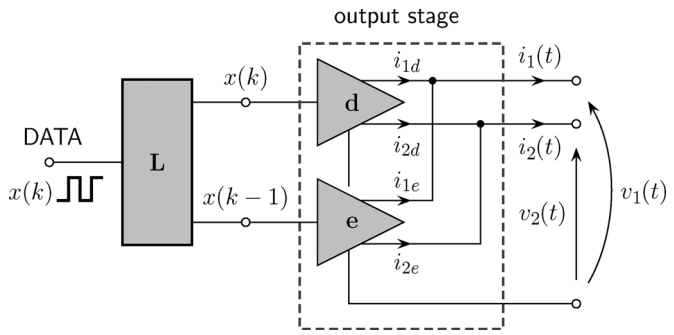

Fig. 2. General structure of a differential driver implementing a FIR filter with two coefficients [see (1)] with the main blocks and the relevant electrical variables.

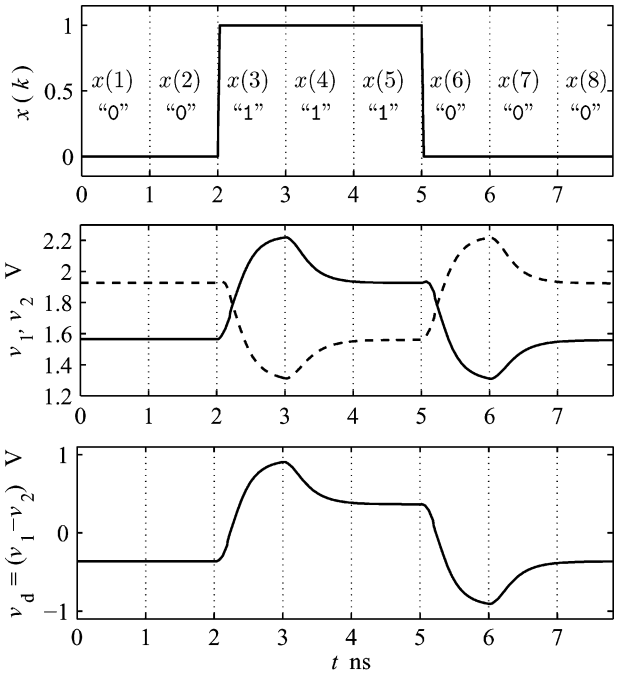

Fig. 3. Example port responses of a differential driver of the type illustrated in Fig. 2.

For implementing the idea of pre-emphasis as shown in the previous example, multisection drivers made of different stages in parallel are employed frequently. Fig. 2 shows an example of such structures with the main blocks and the definition of the electrical variables, for the case of the FIR filter with two coefficients (1). In this structure, $\mathbf{d}$ denotes the main driver and $\mathbf{e}$ a complementary driver providing the user-tunable degree of emphasis. The analog device currents can be expressed as sums of the output currents of the two drivers

$$\begin{cases} i_1 = i_{1d}(t) + i_{1e}(t) \\ i_2 = i_{2d}(t) + i_{2e}(t) \end{cases} \tag{2}$$

where i_{1d}, i_{2d}, and i_{1e}, i_{2e} are the individual contributions of drivers $\mathbf{d}$ and $\mathbf{e}$, respectively. The values of the above currents are decided by the driver's state and strength. The driver's state is controlled by block $\mathbf{L}$, that processes the input bit sequence $x(k)$ to feed drivers $\mathbf{d}$, and $\mathbf{e}$ with $x(k)$ and $x(k-1)$, respectively. Each device current, therefore, is proportional to the signal $a_1 x(k) + a_2 x(k-1)$, where a_1 and a_2 are coefficients taking into account the drivers' strengths. As an example, Fig. 3 shows the output voltage of a driver having the structure of Fig. 2, and producing the bit stream $x(k) =$ "00111000." In each subplot of Fig. 3, the vertical dotted lines indicate the intervals defined by the discrete-time k. More details for this class of devices can be found in [2]–[4].

For the structure of Fig. 2, a behavioral macromodel would be a set of nonlinear dynamic relations approximating the output port currents i_1 and i_2 flowing out of the device port terminals. According to (2), the individual contributions $i_{\alpha d}$ and $i_{\alpha e} (\alpha = 1, 2)$ to the drivers' output currents can be effectively approximated by means of two-piece parametric representations as described in [8]. Thus, the following model representation for the complete driver of Fig. 2 can be adopted (only current i_1 is discussed here for the sake of simplicity)

$$\begin{aligned} i_1 \approx\ & [w_{1dH}(t) i_{1dH}(v_1, v_2, d/dt) + w_{1dL}(t) i_{1dL}(v_1, v_2, d/dt)] \\ & + [w_{1eH}(t) i_{1eH}(v_1, v_2, d/dt) \\ & \quad + w_{1eL}(t) i_{1eL}(v_1, v_2, d/dt)] \end{aligned} \tag{3}$$

where submodels i_{1dH}, i_{1dL} are nonlinear dynamic relations accounting for the behavior of device $\mathbf{d}$ in the fixed high and low state, respectively, and i_{1eH}, i_{1eL} are the corresponding submodels for the driver $\mathbf{e}$. In the previous representation, the w terms are weighting signals accounting for the state transitions of the two output stages (including the appropriate delays).

In principle, a suitable parametric representation for submodels in (3) following the procedure discussed in [8], requires the complete and separate access to each of the two drivers composing the output stage, and this is normally impractical. In order to simplify the modeling procedure, the approximations $i_{1eH} = \alpha_H i_{1dH}$ and $i_{1eL} = \alpha_L i_{1dL}$ are introduced in (3), leading to

$$\begin{aligned} i_1 \approx\ & [w_{1dH}(t) + \alpha_H w_{1eH}(t)]\, i_{1dH} \\ & + [w_{1dL}(t) + \alpha_L w_{1eL}(t)]\, i_{1dL}. \end{aligned} \tag{4}$$

Such a simplification is justified by the similarity of the actual characteristics of real devices. The terms in square brackets in (4), including all the effects of the state transitions of both drivers composing the output stage, can be renamed as new weighting signals w_{1H} and w_{1L} and (4) takes the following form:

$$i_1 \approx w_{1H}(t) i_{1dH}(v_1, v_2, d/dt) + w_{1L}(t) i_{1dL}(v_1, v_2, d/dt). \tag{5}$$

The above representation (5), although derived for the class of differential drivers implementing a FIR filter with two coefficients, is more general and is readily extensible to the case of differential drivers implementing FIR filters with a higher number of coefficients.

III. Macromodel Estimation

The procedure for the estimation of model (5) applies the $M\pi$ log methodology illustrated in [8], since the model structure (5) belongs to the same two-piece representation already developed for the case of plain differential drivers. The objective is to define the nonlinear dynamic submodels i_{1dH} or i_{1dL}, and to compute their parameters and the weighting signals w_{1H} and w_{1L}. The same procedure is applied for the generation of the macromodel accounting for the device behavior of current i_2.

Since the external behavior of *almost any* nonlinear dynamic system can be described as the sum of a possible static part and a dynamic part (see [8, Appendix]), submodel i_{1dH} writes

$$i_{1dH}(v_1, v_2, d/dt) = \hat{i}_{1dH}(v_1, v_2) + \overline{i}_{1dH}(v_1, v_2, d/dt) \quad (6)$$

where $\hat{i}_{1dH}(v_1, v_2)$ is the static characteristic of the device port current i_{1d} and $\overline{i}_{1dH}(v_1, v_2, d/dt)$ is a nonlinear dynamic relationship accounting for the port dynamic behavior, effectively approximated by parametric models. More details on the computation of the static parts and on the parameters estimation of the dynamic parts follow.

The static contribution $\hat{i}_{1dH}(v_1, v_2)$ of (6) is a two-dimensional static surface that can be obtained by means of a set of standard direct current (dc) experiments. In such experiments, the voltage swing applied to the device port terminals should correspond to differential and common mode voltage variations occurring during device operation. The static curves, specified as sampled curves arising from such dc experiments, require to be described by means of analytical expressions in order to facilitate their implementation in a simulation environment. We found that simple piecewise linear interpolations can be effectively used, since most of the simulators have internal keywords for describing sampled static curves. A more sophisticated alternative would consists in approximating the surface by means of sums of local or global basis functions like splines or sigmoidal functions, respectively.

The dynamic contribution $\overline{i}_{1dH}(v_1, v_2, d/dt)$ of (6) is approximated by discrete-time parametric relations involving the present and past samples of input and output variables. Several possible choices can be used for the definition of these relations, ranging from linear models to nonlinear models expressed as sums of nonlinear basis functions [5], [6]. Since a detailed review of parametric models and of their estimation from device port responses is out of the scope of this paper, we refer the reader to [7], [8] where the approach has already been applied to the characterization of single-ended and plain differential devices.

Once the submodels i_{1dH} and i_{1dL} in (5) are completely defined and their parameters estimated, the weighting signals $w_{1H}(t)$ and $w_{1L}(t)$ must be computed by means of the following procedure.

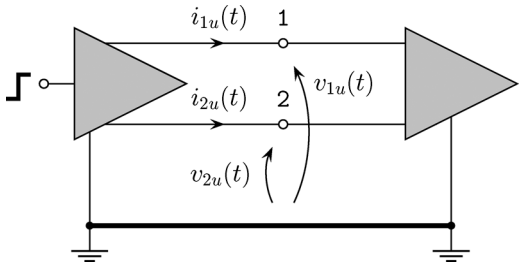

Fig. 4. Test setup for the generation of the transient waveforms used for the computation of the basic weighting coefficients $w_{1H\uparrow}$, $w_{1L\uparrow}$ in (5).

1) The device port voltage and current responses are collected while the driver is connected to one (or more than one) reference load and is forced to produce a single up transition (bit stream "0111...") and a single down transition (bit stream "1000..."). As an example, Fig. 4 shows the test setup for the generation of the port transient responses for the up transition event.
2) The elementary weighting coefficients for up transition ($w_{1H\uparrow}$ and $w_{1L\uparrow}$) and for down transition ($w_{1H\downarrow}$ and $w_{1L\downarrow}$) are computed via linear inversion of the model equation (5) from the device port responses recorded during the previous transition events. For the example setup of Fig. 4, the driver is directly connected to the input port of the transceiver that will be used in a real application of the device. For the sake of simplicity, a single load is considered and the assumption $w_{1L\uparrow} = (1 - w_{1H\uparrow})$ is exploited. Under the above conditions, (5) becomes

$$i_{1u}(t) \approx w_{1H\uparrow}(t) i_{1dH}(v_{1u}, v_{2u}, d/dt) + (1 - w_{1H\uparrow}(t))\, i_{1dL}(v_{1u}, v_{2u}, d/dt) \quad (7)$$

and the sequence of weighting coefficients $w_{1H\uparrow}$ is computed by direct inversion of (7).
3) The complete weighting coefficients w_{1H} and w_{1L} accounting for a specific logic activity of the driver are obtained by means of a juxtaposition in time of the elementary weighting coefficients of up and down transitions, as dictated by the bit sequence (e.g., see Fig. 5, where the basic coefficients are concatenated for the generation of the bit stream "01011000...").

The idealized curves of Fig. 5 along with the proposed model structure (5) highlight that pre-emphasis is accounted for by the overshoots and undershoots of the weighting signals.

IV. Macromodel Implementations

The standard manner of using the models described above in circuit simulation environments, is to convert them into equivalent circuits and to implement them as SPICE-like subcircuits.

Such a conversion and implementation is a standard procedure, and is based on current-controlled sources for the static parts of (6), and on resistance capacitance (RC) networks and controlled sources for the dynamic parts. As an example, Fig. 6 shows the main items of the PSPICE implementation of the proposed macromodel.

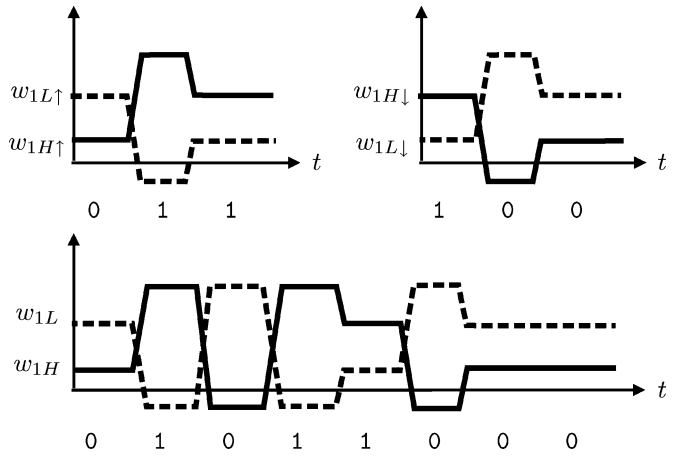

Fig. 5. Example elementary weighting coefficients $w_{1H\uparrow}$ and $w_{1L\uparrow}$ for the up state transition, and $w_{1H\downarrow}$ and $w_{1L\downarrow}$ for the down state transition (top left and right panel, respectively). Weighting coefficients w_{1H} and w_{1L}, obtained as juxtaposition of the elementary weighting coefficients for the generation of the bit pattern "01011000" are shown in the lower panel.

```
.subckt driverX 1 2 ref
.PARAMS
+ alpha11H= ...
+ alpha12H= ...
...
+ alpha11L= ...
+ alpha12L= ...
...
* output controlled sources
  G1 ref 1 value={V(w1H,ref)*(V(n1H,ref)+V(n1Hhat,ref)))
  + + V(w1L,ref)*(V(n1L,ref)+V(n1Lhat,ref)))}
  G2 ref 2 value={V(w2H,ref)*(V(n2H,ref)+V(n2Hhat,ref)))+
  + + V(w2L,ref)*(V(n2L,ref)+V(n2Lhat,ref)))}
* port voltage derivatives
  Ev1dot ref v1dot ref value={V(1,ref)}
  Cv1dot v1dot ref 1
  Ev2dot ref v2dot ref value={V(2,ref)}
  Cv2dot v2dot ref 1
* static characteristics
  R1Hhat n1Hhat ref 1
  E1Hhat n1Hhat ref value={
  * analytical expression of static characteristic
   ...
  + }
  R1H n1H ref 1
  E1H n1H ref value={alpha11H*I(Ev1dot)+alpha12H*I(Ev2dot)}
  ...
* weighting coefficients
  Rw1H w1H ref
  Ew1H w1H ref PWL(
  + 0 0
  + ...
  )
  ...
.ends
```

Fig. 6. PSPICE implementation of the driver macromodel (5).

```
entity driverX is
generic (
  alpha11H:=...
  ...

port(
  d_control :  in std_logic;
  terminal a_signal_pos, a_signal_neg :  electrical);
end entity driverX;

architecture bufferbehav of driverX is
-- quantity declaration:
  quantity v1 across i1 through a_signal_pos to Electrical_ref;
  quantity v2 across i2 through a_signal_neg to Electrical_ref;
-- constant declaration
   constant tw :  real_vector := ...
   constant w1H_up :  real_vector := ...
...
function Lookup (...
...
end function Lookup;

-- PROCESS STATEMENT FOR THE D/A CONVERSION
-----------------------------------------------------------
-- i.e.  juxtaposition of the basic weighting coeff.
begin
process (d_control)
begin
if (d_control'event and d_control = '0'
and domain /= quiescent_domain) then
  -- Transition DOWN
     transition <= 10;
elsif (d_control'event and d_control = '1'
and domain /= quiescent_domain ) then
  -- Transition UP
     transition <= 01;
end if;
instant_front <= now;
end process;

--- ANALOG EQUATIONS
-----------------------------------------------------------
if (transition = 10) use -- d_control = '0'
   w1H == Lookup("Vt", now-instant_front, w1H_down, tw);
   ...
elsif (transition = 01) use -- d_control = '1'
   w1H == Lookup("Vt", now-instant_front, w1H_up, tw);
   ...
end use;
i1Hhat == ...
...
i1H == i1Hhat + alpha11H*v1'dot + alpha12H*v2'dot;
i1L == i1Lhat + alpha11L*v1'dot + alpha12L*v2'dot;
i2H == i2Hhat + alpha21H*v1'dot + alpha22H*v2'dot;
i2L == i2Lhat + alpha21L*v1'dot + alpha22L*v2'dot;
i1 == (w1H*i1H + w1L*i1L);
i2 == (w2H*i2H + w2L*i2L);
end architecture bufferbehav;
```

Fig. 7. VHDL-AMS implementation of macromodel (5). Some example templates we used for the D/A conversion are posted on http://www.eda.org/pub/ibis/summits/jun03a/ and http://www.eda.org/pub/ibis/summits/feb04a/.

It is worth noting that the basic keywords available in most SPICE-type simulators do not allow to easily implement the juxtaposition of the elementary weighting coefficients of the up and the down transitions shown in Fig. 5. Owing to this, the voltage sources implementing the weighting coefficients in (5), are best computed offline for a predetermined bit pattern (e.g., see the Ew1H statement in the netlist of Fig. 6). On the other hand, the recent interest and availability of integrated analog mixed-signal simulation tools, drove the attention to other possible model descriptions via metalanguages like Verilog-AMS or VHDL-AMS. Such languages greatly facilitate the implementation of the juxtaposition of the elementary weighting sequences, since they include commands for logical operations. A detailed description of the VHDL-AMS language is out of the scope of this paper and can be found in [15] and [16]. However, as a

TABLE I
FILE SIZES OF TWO DIFFERENT DRIVER MACROMODEL IMPLEMENTATIONS FOR A DIFFERENT LENGTH OF THE BIT PATTERN

# bits	PSPICE	VHDL-AMS
256	3.1 MB	193 kB
512	4.6 MB	
1024	7.5 MB	
2048	13.2 MB	

simple example higlighting the strenghts of the VHDL-AMS code, Fig. 7 shows the main part of the AMS implementation of the driver macromodel. In this code, the types of macromodel ports (e.g., electrical or digital ports) are defined by means of the keyword `port` within the `entity` section. Section `architecture`, instead, collects all the variables, equations and auxiliary functions needed for the model definition. In addition, keyword `quantity` allows the definition of other variables like the associated port voltages and currents for the two output pins of the differential driver. The juxtaposition of the elementary weighting coefficients is simply carried out within the section starting with keyword `process` (D/A conversion) by sensing the present bit at the logical port `D_digital`. The last part of the code implements the analog equations of the macromodel. As a final remark arising from the different implementations of the weighting signals in different languages, Table I collects the file sizes of the proposed driver macromodel implemented in both PSPICE and VHDL-AMS for a different length of the bit pattern. From this table, the great advantage of using VHDL-AMS for the real-time generation of the weighting signals can be clearly appreciated, since the capability of AMS to handle the processing of logic variables leads to a file size independent of the bit pattern length.

Finally, it is worth noting that most commercial tools for SI/EMC adopt an input output buffer information specification (IBIS) description of devices as a standard way for the inclusion of IC port models into the tool. IBIS is a well established standard for the definition of IC models by means of simplified equivalent circuits [12], leading to a large availability of device descriptions. Recently, the growing complexity of devices and their enhanced features like pre-emphasis, demands for refinements of the basic equivalent circuits and for the availability of different models. Owing to this, starting with version 4.1, the IBIS standard allows for the inclusion of external user-defined models in different possible languages like SPICE or VHDL-AMS, enabling different user-defined models in most EDA tools. Within this framework, our methodology can be effectively used and the models directly plugged into the IBIS definition of a digital IC. A sample template of an IBIS file describing a digital circuit collecting a plain differential driver defined by an external VHDL-AMS description like the one in Fig. 7 is included in [8].

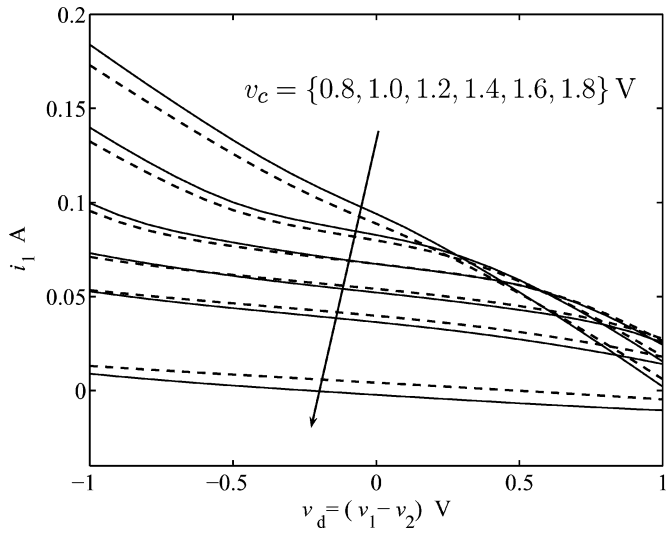

Fig. 8. Static characteristics of the current $i_1 = i_{1dH} + i_{1eH}$ flowing out of the first terminal of the example driver while the two internal drivers are forced in the fixed High output state. Solid curves represent the reference charactersitics, while the curves obtained by means of the approximation $i_{1eH} = \alpha_H i_{1dH}$ are shown as broken lines.

V. APPLICATION EXAMPLE

In this section, the proposed modeling approach is demonstrated for a Xilinx multigigabit serial transceiver used in the Virtex-II Pro series FPGA. The example transceiver is a differential current mode logic (CML) device operating in the frequency range 622 Mb/s–3.125 Gb/s and allowing a configurable degree of pre-emphasis within the range 10%–33%. The internal structure of the output buffer of the example transceiver, available as a detailed HSPICE transistor-level from the official Xilinx website[1], is used as the *reference* model hereafter. In all tests carried out in this study, the reference model with a $\beta = 33\%$ degree of pre-emphasis is used to compute the responses needed for the estimation of macromodel parameters and for model validations. More details on the device and on the usage of the reference model can be found in [17].

For the macromodel generation, piecewise linear interpolations are used to approximate the static characteristics like $\hat{i}_{dH}$ of (6) and simple linear auto regression with eXtra input (ARX) parametric models are used for the dynamic parts like in $\overline{i}_{dH}$ of (6) (as already done for the characterization of plain differential devices in [8]). The weighting signals and submodel parameters are computed by means of the procedure outlined in the previous section and the obtained macromodels are implemented in both VHDL-AMS and SPICE.

The accuracy of the proposed macromodels has been quantified by computing the timing error and the maximum relative voltage error. The timing error is defined as the maximum delay between the reference and the macromodel responses measured for the zero voltage crossing of the differential voltage $v_d = v_1 - v_2$. The maximum relative voltage error is computed as the maximum error between the reference and macromodel voltage responses divided by the voltage swing.

[1]www.xilinx.com

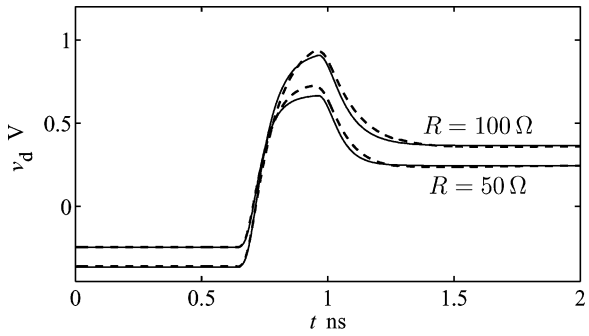

Fig. 9. Differential voltage $v_d(t)$ computed for the example driver producing a bit stream "0111. . .." The driver is loaded by a simple differential resistor R. Solid curves: reference. Dashed curves: macromodel.

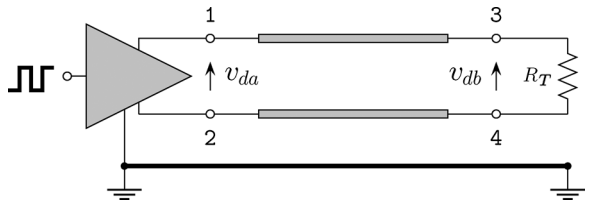

Fig. 10. Application test case: a high-speed data communication link with the relevant electric variables (see text for details).

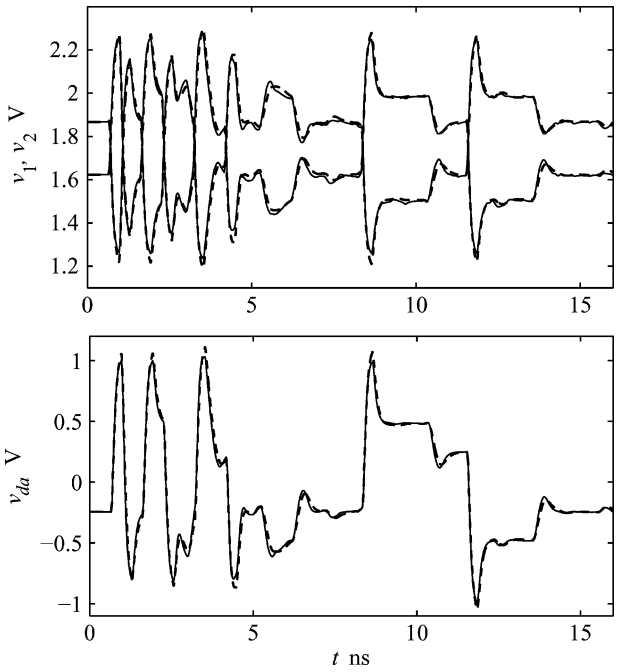

Fig. 11. Output port voltages $v_1(t)$, $v_2(t)$ (top panel) and differential voltage $v_{da}(t)$ (bottom panel) computed for the example driver used in the configuration of Fig. 10. Solid line: reference. Dashed line: macromodel.

In order to verify the simplifying assumption of dealing with devices in which the characteristic of the tap driver $\mathbf{e}$ is roughly proportional to the characteristic of the main driver $\mathbf{d}$, Fig. 8 shows the static characteristic of the current $i_1 = i_{1dH} + i_{1eH}$ flowing out of the first terminal of the example driver while the two internal drivers are forced in the fixed high output state. In this figure, the curves are the actual static characteristic of the driver superimposed on the approximating curves obtained by means of the simplifying assumption $i_{1eH} = \alpha_H i_{dH}$, where the value of the linear coefficient α_H has been estimated offline to be 0.08. All curves are computed for different values of the common and differential mode voltages v_d and $v_c = (v_1 + v_2)/2$. Fig. 8 shows some unavoidable differences between the true characteristics and the approximated curves, with a maximum relative errors on the order of 4%. It is worth mentioning that these differences are partly compensated by the weighting coefficients in the complete model, that are obtained by minimizing the error between reference and model response.

The first validation is devised to highlight the accuracy of the macromodel for loads different from those used in the estimation process: we consider a test setup consisting of the example driver connected to a 50 Ω and to a 100 Ω differential resistors. The driver is forced to produce a "0111..." bit stream. In the estimation procedure, model parameters were obtained from the transient responses of the driver connected to the transceiver input section, as shown in Fig. 4. Fig. 9 shows the differential voltage waveform $v_d(t)$ computed by the reference model and by the PSPICE implementation of the macromodel. In this test, the timing error is 5 ps (1.6% of bit time) and the maximum relative error is less than 5%.

In the second validation, the driver is connected to a coupled interconnect structure, as shown in Fig. 10. The interconnect is a lossless symmetric transmission line (even mode impedance $Z_e = 90\ \Omega$, odd mode impedance $Z_o = 50\ \Omega$, line length 0.30 m) loaded by a $R_T = 50\,\Omega$ differential resistor. The data pattern used for this study is a 2048 bit-long sequence with 0.32 ns bit time (3.125 Gb/s) and a jitter error uniformly distributed in the range [−35, 35] ps. For this test case, Fig. 11 shows the reference and macromodel responses of the port voltages $v_1(t)$ and $v_2(t)$ and of the near-end differential voltage $v_{da}(t)$, for a duration of 16 ns, picked at random along the simulation of the entire bit pattern. The macromodel response is obtained either by using the HSPICE and the VHDL-AMS implementations of the macromodel. Also in this case, a good agreement between reference and predicted signals is obtained, with timing errors on the order of 5 ps (1.6% of bit time) and maximum relative voltage errors less than 3% of voltage swings. In order to better quantify the maximum errors in the complete predicted sequence, the complete eye diagrams derived from both the reference and the model responses of the far-end differential voltage $v_{db}(t)$ are compared, as shown in Fig. 12. Such a comparison is done by computing the eye apertures ΔT and ΔV defined as in Fig. 12. Plots of ΔT versus ΔV are shown in Fig. 13, where, for every value of ΔV, the difference of the corresponding ΔT's quantifies the error in the eye opening caused by the use of approximate waveforms. This comparison highlights that the openings of eye diagrams obtained from simulations with macromodels are within 1 / 2% of openings from reference simulations of the entire 2048 bit long sequence.

The efficiency gain of the proposed macromodels with respect to the original transistor level models depends on two factors: the implementation of the logical block $\mathbf{L}$ and the complexity of the analog driver devices. Analog implementations of $\mathbf{L}$, as in conventional transistor-level models, requires a run-in time delay for proper operation. As an example, the run-in time

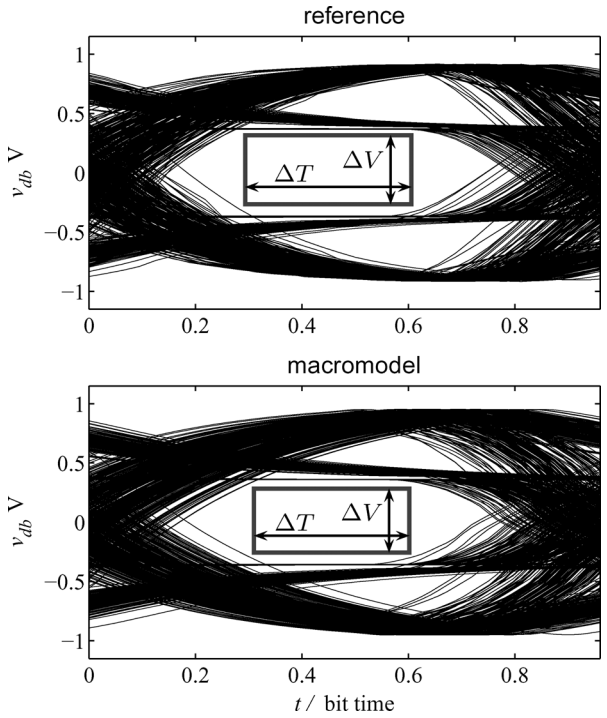

Fig. 12. Eye diagram arising from the reference and predicted waveforms $v_{db}(t)$ of the test case of Fig. 10 and definition of the eye opening parameters ΔV and ΔT.

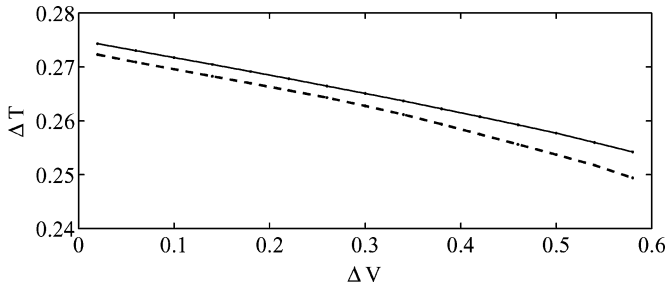

Fig. 13. Relationship between the two eye opening parameters defined in Fig. 12 for the voltage $v_{db}(t)$. Solid thin line: reference. Dashed thick line: macromodels.

of the transistor-level model of the device of this study is 150 ns (i.e., approximately 500 clock cycles at 3.125 Gb/s), which considerably increases simulation times. On the contrary, the proposed macromodel automatically includes the role of the logical block into the weighting signals of (5), thus avoiding, even in a SPICE-like implementation, the overhead of the run-in time. The efficiency gain for the analog driver components, instead, compares to that allowed by the $\mathrm{M}\pi\log$ approach for conventional devices, i.e., speedup factors on the order of 5 / 100 are possible.

As a final remark, it is worth noting that the weighting coefficients w_{1H} and w_{1L} of (5) can be easily parametrized in order to account for the effects of the user tunable degree of pre-emphasis β. In fact, the weighting signals are the dominant elements to include the effects of the strength of the complementary driver e. They automatically hide the linear coefficients α_H and α_L used for the simplifying assumption leading to the proposed model equation (5). Since different values of β modify the

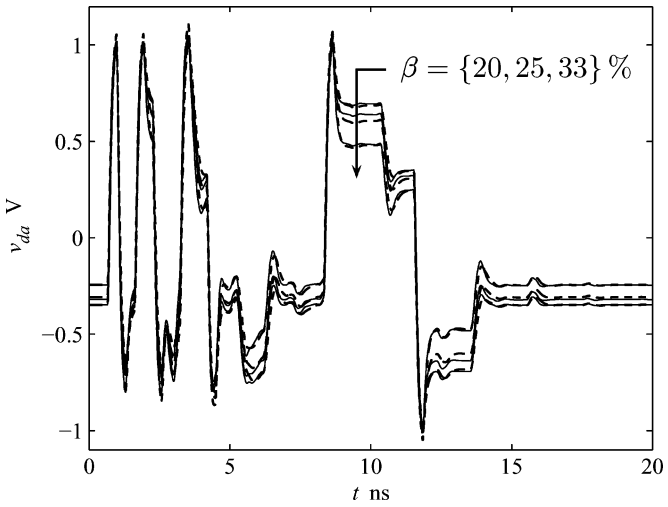

Fig. 14. Differential voltage $v_{da}(t)$ computed for the example driver used in the configuration of Fig. 10, with different pre-emphasis percentages β. Solid line: reference. Dashed line: macromodel.

values of the α_H and α_L, such a variation can be seen simply as a variation of the weighting signals. As an example, once the submodels i_{1dH} and i_{1dL} are estimated for the case of the driver with $\beta = 33\%$ as in the previous test cases, two different sets of weighting coefficients can be estimated from the driver port transient response recorded while the device is set to two different values of β (e.g., $\beta = 10\%$ and $\beta = 33\%$). The weighting signals for an arbitrary value of β can be then computed as a weighted sums of the previous two sets of signals. Fig. 14 shows the differential voltage waveform $v_{da}(t)$ computed by the reference transistor-level model of the driver and by the macromodel. The same application test case of Fig. 10 and different values of β are considered. The curves prove that the important parameter defining the degree of pre-emphasis is readily available in the proposed macromodel as in the original transistor-level description of device.

VI. Conclusion

This paper addresses the macromodeling of differential drivers with pre-emphasis for the assessment of signal integrity and electromagnetic compatibility effects in multi-gigabit data transmission systems. A suitable model structure based on parametric relations is derived and the procedure for parameter estimation is outlined. Model parameters can be easily estimated from device port responses only. Besides, the obtained models can be easily implemented in any EDA tool supporting the IBIS 4.1 specification for digital ICs or accepting SPICE or metalanguage descriptions. The models have been proven to be accurate and efficient enough for the performance predictions in multigigabit applications.

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